CLAIMS

What is claimed is:

1. A microelectronic product comprising:

a substrate having exposed therein a first contact region and a second contact region;

a first dielectric layer formed over the substrate and a second dielectric layer formed over the first dielectric layer;

a capacitor formed interposed between the first dielectric layer and the second dielectric layer, the capacitor also being sandwiched between a first conductor stud that penetrates the first dielectric layer and contacts the first contact region and a second conductor stud that penetrates the second dielectric layer; and

a contiguous conductor interconnect and conductor stud layer contacting the second contact region and formed into a trench defined within the second dielectric layer and a contiguous via defined within the first dielectric layer.

2. The microelectronic product of claim 1 further comprising an etch stop layer interposed between the first dielectric layer and the second dielectric layer.

3. The microelectronic product of claim 2 wherein the etch stop layer simultaneously serves as a floor of the trench and passivates a sidewall of the capacitor.

4. The microelectronic product of claim 3 wherein at least one of the first dielectric layer and the second dielectric layer is formed of a comparatively low dielectric constant dielectric material.

5. The microelectronic product of claim 4 wherein the etch stop layer is formed of a silicon nitride material.

6. The microelectronic product of claim 1 further comprising a spacer layer passivating a sidewall of the capacitor.

7. A microelectronic product comprising:

a substrate having exposed therein a first contact region and a second contact region;

a first dielectric layer formed over the substrate and a second dielectric layer formed over the first dielectric layer;

a capacitor formed interposed between the first dielectric layer and the second dielectric layer, the capacitor also being sandwiched between a first conductor stud that penetrates the first dielectric layer and contacts the first contact region and a second conductor stud that penetrates the second dielectric layer;

a spacer layer passivating a sidewall of the capacitor; and

a contiguous conductor interconnect and conductor stud layer contacting the second contact region and formed into a trench defined within the second dielectric layer and a contiguous via defined within the first dielectric layer, wherein the trench has as its floor an etch stop layer

interposed between the first dielectric layer and the second dielectric layer and also passivating a sidewall of the capacitor.

8. The microelectronic product of claim 7 wherein the substrate comprises a semiconductor substrate.

9. The microelectronic product of claim 7 wherein at least one of the first dielectric layer and the second dielectric layer is formed of a comparatively low dielectric constant dielectric material.

10. The microelectronic product of claim 7 wherein the spacer layer is formed of a silicon oxide material.

11. The microelectronic product of claim 7 wherein the etch stop layer is formed of a silicon nitride material.

12. The microelectronic product of claim 7 wherein etch stop layer is formed upon the spacer layer and passivating the sidewall of the capacitor.

13. A method for fabricating a microelectronic product comprising:

providing a substrate having exposed therein a first contact region and a second contact region;

forming a first dielectric layer over the substrate and a second dielectric layer over the first dielectric layer;

forming a capacitor interposed between the first dielectric layer and the second dielectric layer, where the capacitor is also formed sandwiched between a first conductor stud that penetrates the first dielectric layer and contacts the first contact region and a second conductor stud that penetrates the second dielectric layer; and

forming a contiguous conductor interconnect and conductor stud layer contacting the second contact region and into a trench defined within the second dielectric layer and a contiguous via defined within the first dielectric layer.

14. The method of claim 13 further comprising forming an etch stop layer interposed between the first dielectric layer and the second dielectric layer.

15. The method of claim 14 wherein the etch stop layer simultaneously serves as a floor of the trench and passivates a sidewall of the capacitor.

16. The method of claim 15 wherein at least one of the first dielectric layer and the second dielectric layer is formed of a comparatively low dielectric constant dielectric material.

17. The method of claim 16 wherein the etch stop layer is formed of a silicon nitride material.

18. The method of claim 13 further comprising forming a spacer layer passivating a sidewall of the capacitor.

19. The method of claim 13 wherein a second via into which is formed the second stud is formed in part simultaneously with the via contiguous with the trench.

20. The method of claim 13 wherein the second stud is formed simultaneously with the contiguous conductor interconnect and conductor stud layer.